DETAILED ACTION

This application has been examined. Claims 1-19,21-30 are pending. Claim 20 is cancelled.

Making Final

Applicant's arguments filed 03/03/2009 have been fully considered but they are not persuasive.

The claim amendments regarding -- '*the manageability control module configured to apply a protocol for communicating over the microprocessor bus system*' -- and -- '*the manageability control module configured to provide access for allowing another microprocessor subsystem to perform the management function even when the processor core is not responsive*' -- do not overcome the disclosure by the prior art as shown below.

The Examiner is maintaining the rejection(s) using the same grounds for rejection and thus making this action FINAL.

Response to Arguments

Applicant's arguments filed 03/03/2009 have been fully considered but they are not persuasive.

The Applicant presents the following argument(s) [*in italics*]:

… Narasimhan does not teach or render obvious the management block including a manageability control module configured to apply a protocol for communicating over the microprocessor bus system, and configured to provide access for allowing another microprocessor subsystem to perform the management function even when the processor core is not responsive.

The Examiner respectfully disagrees with the Applicant.

Narasimhan disclosed (re. Claim 1) wherein the management block includes a *manageability control module configured to apply a protocol for communicating over the microprocessor bus system* (Narasimhan-Column 14 Lines 5-15, Column 17 Lines 25-30,*'the protocol operates over a serial or parallel bus interface'*) *and the manageability control module configured to provide access for allowing another microprocessor subsystem to perform the management function even when the processor core is not responsive.* (Narasimhan-Column 14 Lines 40-50,*'NIC will support external Direct Memory Access, providing an interface for a DMA controller thus allowing read/write commands into device registers'*)

The Examiner interprets the management function as per Applicant Specification Page 10 Lines 15-25, wherein the management function is for accessing memory.

The Examiner further notes that Narasimhan supports devices without a CPU or microcontrollers, and thus obviates requiring responsive processor cores on the device.

Priority

The effective date of the claims described in this application is March 29, 2004.

Information Disclosure Statement

The Applicant is respectfully reminded that each individual associated with the filing and prosecution of a patent application has a duty of candor and good faith in dealing with the Office, which includes a duty to disclose to the Office all information known to that individual to be material to patentability as defined in 37 CFR 1.56.

There were no information disclosure statements filed with this application.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-11, 14-18, 28-30 rejected under 35 U.S.C. 103(a) as being unpatentable over Narasimhan (US Patent 6446192) in view of Bishop (US Patent 4914653).

Narasimhan disclosed (re. Claim 1) a management port for a wireless device platform, comprising: a communication link (Narasimhan-Figure 7 , Column 6 Lines 30-35, '*network interface chip'*) for the wireless device platform, (Narasimhan-Column 3 Lines 15-20) the communication link to provide an inbound link and an outbound link, (Narasimhan-Column 13 Lines 40-50) and to control data flow over the inbound and outbound links; and

a management block to receive command data *from the at least one processor or peripheral* through a predetermined logic channel in the inbound link, the management (Narasimhan-Figure 7, '*command processor*') through a channel in the inbound link and generate a corresponding command signal on a microprocessor bus system (Narasimhan-Figure 9,Column 13 Lines 55-65, Column 14 Lines 30-35) that is local to the command link to perform a management function for the microprocessor system, (Narasimhan- Column 14 Lines 30-35,'*microcontroller'*) the management block being further adapted to receive a response signal from the bus and transmit corresponding response data through a channel in the outbound link. (Narasimhan-Column 13 Lines 40-50)

Narasimhan disclosed (re. Claim 1) a communication link, local to a microprocessor subsystem. (Narasimhan-Figure 2,Column 14 Lines 30-35,*'the internal data bus of the NIC connects directly to the device data bus*').

Narasimhan disclosed (re. Claim 1) the microprocessor subsystem comprising a processor core and at least one processor subsystem, and a microprocessor bus system, (Narasimhan-Figure 9,Column 13 Lines 55-65, Column 14 Lines 30-35) the microprocessor bus system providing a communication path between the processor core and the at least one processor subsystem; (Narasimhan-Figure 9)

Narasimhan disclosed (re. Claim 1) the inbound link providing a path for communications from the inter- processor bus to a peripheral bus (Narasimhan-Column 14 Lines 25-35) of the microprocessor subsystem, the inbound link receiving communications from at least one processor or peripheral communicating over the inter-processor bus, (Narasimhan-Column 13 Lines 40-50)

the outbound link providing a path for communications from the peripheral bus of the microprocessor subsystem to the inter-processor bus, (Narasimhan-Column 14 Lines 25-35) the outbound link transmitting communications over the inter-processor bus to the at least one processor or peripheral, (Narasimhan-Column 13 Lines 40-50)

Narasimhan disclosed (re. Claim 1) wherein the management block includes a *manageability control module configured to apply a protocol for communicating over the microprocessor bus system* (Narasimhan-Column 14 Lines 5-15, Column 17 Lines 25-30,*'the protocol operates over a serial or parallel bus interface'*) *and the manageability control module configured to provide access for allowing another microprocessor subsystem to perform the management function even when the processor core is not responsive.* (Narasimhan-Column 14 Lines 40-50,*'NIC will support external Direct Memory Access, providing an interface for a DMA controller thus allowing read/write commands into device registers'*)

The Examiner interprets the management function as per Applicant Specification Page 10 Lines 15-25, wherein the management function is for accessing memory.

The Examiner further notes that Narasimhan supports devices without a CPU or microcontrollers, and thus obviates requiring responsive processor cores on the device.

While Narasimhan substantially disclosed the claimed invention Narasimhan did not disclose (re. Claim 1) inter-processor communication and using logic channels.

Bishop disclosed (re. Claim 1) inter-processor communication and using logic channels. (Bishop-Column 6 Lines 55-65)

Narasimhan and Bishop are analogous art because they present concepts and practices regarding interfaces for multi-processor systems. At the time of the invention

it would have been obvious in the networking art to combine Bishop into Narasimhan. The motivation for said combination would have been to minimize latency (Bishop-Column 2 Lines 15-20).

Claims 8,15,28 are rejected on the same basis as Claim 1.

Narasimhan-Bishop disclosed (re. Claim 28) the multi-channel (Bishop-Column 6 Lines 55-65) inbound link providing a path for communications from the inter-processor bus to a peripheral bus of the microprocessor system, (Narasimhan-Column 13 Lines 40-50) the multi-channel inbound link receiving communications from at least one processor or peripheral communicating over the inter-processor bus, (Narasimhan-Column 14 Lines 25-35)

the multi-channel (Bishop-Column 6 Lines 55-65) outbound link providing a path for communications from the peripheral bus of the microprocessor system to the inter-processor bus, (Narasimhan-Column 13 Lines 40-50) the multi- channel outbound link transmitting communications over the inter-processor bus to the at least one processor or peripheral; (Narasimhan-Column 14 Lines 25-35)

Narasimhan-Bishop disclosed (re. Claim 2,17,29) wherein the communication link includes a physical layer to provide both the inbound and outbound links (Narasimhan-Column 13 Lines 40-50) with multiple logic channels, (Bishop-Column 6

Lines 55-65) and a data link protocol to control data flow over the inbound and output links, (Narasimhan-Column 13 Lines 40-50) and

the management block provides the corresponding command signal directly on the microprocessor bus. (Narasimhan-Column 14 Lines 25-35)

Narasimhan-Bishop disclosed (re. Claim 3,9) wherein the management function includes a debug function. (Narasimhan-Column 1 Lines 20-25,Column 14 Lines 60-65,'*STATUS registers provide information about errors'*)

Narasimhan-Bishop disclosed (re. Claim 4,10) wherein the management function includes accessing memory. (Narasimhan-Column 17 Lines 45-55, '*the variable is identified and the device processor writes the value to the network interface chip'*)

Narasimhan-Bishop disclosed (re. Claim 5,11) wherein the management function includes accessing configuration registers. (Narasimhan-Column 16 Lines 55-65)

Narasimhan-Bishop disclosed (re. Claim 6) wherein the management function includes accessing a peripheral device of the microprocessor system. (Narasimhan-Column 14 Lines 20-25,*'other device peripherals*')

Narasimhan-Bishop disclosed (re. Claim 7,16,30) wherein the management block includes: a command register connected to the bus and to the communication link, (Narasimhan-Column 14 Lines 60-65,*'commands are written to the WRITE DATA register'*) the command register to temporarily store the command data delivered through the predetermined logic channel in the inbound link; a response register connected to the bus and to the communication link, the response register to temporarily store response data from the bus; (Narasimhan-Column 14 Lines 60-65,*'received data are read from the READ data register'*) and a manageability controller connected to the microprocessor bus, the command register, and the response register, the manageability controller (Narasimhan-Column 6 Lines 30-40) being adapted to determine when command data is received at the command register and to transmit the corresponding command signal over the bus, and further being adapted to receive the response signal from the bus and store corresponding response data at the response register, and to transmit the response data through the predetermined logic channel in the outbound link.(Narasimhan-Figure 7,Column 13 Lines 40-50)

Narasimhan-Bishop disclosed (re. Claim 14) the management block being adapted to generate the corresponding command signal on the at least one bus to perform a management function for the at least one peripheral device. (Narasimhan-Column 6 Lines 30-40)

Narasimhan-Bishop disclosed (re. Claim 18) wherein the embedded communications microprocessor system is adapted to wirelessly communicate with at least one other devices. (Narasimhan-Column 3 Lines 15-20)

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 12,13, 19,21-27 rejected under 35 U.S.C. 103(a) as being unpatentable over Narasimhan (US Patent 6446192) in view of Bishop (US Patent 4914653) further in view of Balachandran (US Publication 20050078620).

Narasimhan-Bishop disclosed (re. Claim 19) an inter-processor communication bus connected to the communication links of both the applications microprocessor system and the communications microprocessor system, as disclosed in the rejection for Claim 1.

Furthermore Narasimhan-Bishop disclosed (re. Claim 19) the inbound link providing a path for communications from the inter- processor bus to a peripheral bus (Narasimhan-Column 14 Lines 25-35) of the microprocessor subsystem, the inbound link receiving communications from at least one processor or peripheral communicating over the inter- processor bus, (Narasimhan-Column 13 Lines 40-50)

the outbound link providing a path for communications from the peripheral bus of the microprocessor subsystem to the inter-processor bus, (Narasimhan-Column 14 Lines 25-35) the outbound link transmitting communications over the inter-processor bus to the at least one processor or peripheral, (Narasimhan-Column 13 Lines 40-50)

Furthermore Narasimhan-Bishop disclosed (re. Claim 19) a manageability port: being adapted to receive command data from the at least one processor or peripheral through a predetermined logic channel in the inbound link,
providing a corresponding command signal on the microprocessor bus, and further is adapted to receive a response signal from the microprocessor bus, and
transmitting corresponding response data through a predetermined logic channel in the outbound link to the at least one processor or peripheral via the inter-processor bus. (see rejection for Claim 1)

While Narasimhan-Bishop substantially disclosed the claimed invention Narasimhan-Bishop did not disclose (re. Claim 19) a substantially omni-directional antenna connected to the embedded communications microprocessor system; (re. Claim 12) wherein the at least one processor subsystem includes a security module; (re. Claim 13) wherein the at least one processor subsystem includes a Universal Serial Bus (USB) client

Balachandran disclosed (re. Claim 19) a substantially omni-directional antenna connected to the embedded communications microprocessor system. (Balachandran-Paragraph 8 Figure 1)

Balachandran disclosed (re. Claim 12) wherein the at least one processor subsystem includes a security module (Balachandran-Paragraph 50)

Balachandran disclosed (re. Claim 13) wherein the at least one processor subsystem includes a Universal Serial Bus (USB) client. (Balachandran-Paragraph 33, Figure 4)

Narasimhan,Bishop and Balachandran are analogous art because they present concepts and practices regarding interfaces for multi-processor systems. At the time of the invention it would have been obvious in the networking art to combine Balachandran into Narasimhan-Bishop. The motivation for said combination would have been to

enable separation of the access functionality and the application functionality as implemented in two separate processors. (Balachandran-Paragraph 32)

Narasimhan-Bishop-Balachandran disclosed (re. Claim 21) wherein the embedded communications microprocessor system includes a microprocessor system adapted to wirelessly communicate with at least one other device. (Narasimhan-Column 3 Lines 15-20)

Narasimhan-Bishop-Balachandran disclosed (re. Claim 22) wherein the microprocessor system is adapted to wirelessly communicate with at least one other devices using IEEE 802.11 technology. (Balachandran-Paragraph 33, Figure 4)

Narasimhan-Bishop-Balachandran disclosed (re. Claim 23) wherein the microprocessor system is adapted to wirelessly communicate with at least one other device using cellular radio technology. (Balachandran-Paragraph 33, Figure 4)

Narasimhan-Bishop-Balachandran disclosed (re. Claim 24) wherein the microprocessor is adapted to wirelessly communicate using general packet radio service (GPRS) technology. (Balachandran-Paragraph 33, Figure 4)

Narasimhan-Bishop-Balachandran disclosed (re. Claim 25) wherein the microprocessor is adapted to wirelessly communicate using code division multiple access (CDMA) technology. (Balachandran-Paragraph 35, '*standard wireless technologies*')

Narasimhan-Bishop-Balachandran disclosed (re. Claim 26) wherein the microprocessor is adapted to wirelessly communicate using wideband code division multiple access (WCDMA) technology. (Balachandran-Paragraph 35, '*standard wireless technologies*')

Narasimhan-Bishop-Balachandran disclosed (re. Claim 27) a microprocessor system adapted to wirelessly communicate with at least one other devices using an IEEE 802.11 technology; and a microprocessor system adapted to wirelessly communicate with at least one other device using cellular radio technology. (Balachandran-Paragraph 33, Figure 4)

Conclusion

Examiner's Note: Examiner has cited particular columns and line numbers in the references applied to the claims above for the convenience of the applicant. Although the specified citations are representative of the teachings of the art and are

applied to specific limitations within the individual claim, other passages and figures may apply as well. It is respectfully requested from the applicant in preparing responses, to fully consider the references in entirety as potentially teaching all or part of the claimed invention, as well as the context of the passage as taught by the prior art or disclosed by the Examiner.

In the case of amending the claimed invention, Applicant is respectfully requested to indicate the portion(s) of the specification which dictate(s) the structure relied on for proper interpretation and also to verify and ascertain the metes and bounds of the claimed invention.

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Greg Bengzon whose telephone number is (571) 272-3944. The examiner can normally be reached on Mon. thru Fri. 8 AM - 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, William Vaughn can be reached on (571)272-3922. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/G. B./
Examiner, Art Unit 2444

/William C. Vaughn, Jr./

Supervisory Patent Examiner, Art Unit 2444